IN THE SPECIFICATION

Please amend as follows the paragraph starting at page 2, line 26 :

The teachings of the first two classes of embodiments of the invention are equally applicable to both RFID tags and smart cards with RF transponder/processor/memory circuits integrated directly onto the same plastic substrate on which the antenna is formed. Typically the antenna will have two terminals for connection to the RF input/output terminals of the integrated circuit, but in some embodiments, there may be only one terminal for the antenna that is connected directly to the IC with the other terminal connected to a ground plane of conductive material formed on the plastic substrate with the IC having one RF I/O terminal coupled to the antenna and the other coupled to the ground plane. The phrase "integrated on" as used in the claims means an integrated circuit that is formed directly on the plastic substrate by processing the plastic substrate in flat panel display manufacturing or other semiconductor wafer processing machines used for making integrated circuits. The phrase "bonded or <u>otherwise</u> ~~otherwised~~ attached to" is intended to describe a plastic substrate upon which is bonded an integrated circuit made on another glass or plastic substrate elsewhere which is then diced and bonded or otherwise physically attached to the plastic substrate.

Please amend as follows the paragraph starting at page 11, line 16:

Figure 2 represents a process flow to make the structure of Figure 1. Note that Figure 1 shows only a single self-aligned thin film MOS transistor whereas the RFID tag requires that a data processor section, a memory section and an RF transceiver circuit all be integrated into the IC. Since the actual circuitry of the RFID transceiver is not part of the invention, this disclosure will

focus only on the processes and structures of fully integrated RFID tags for the first class of embodiments and RFID tags constructed by the "cut and paste" method using transceiver ICs that have been manufactured cheaply using flat panel display processes. Figures 1 and 2 represents examples of the structure and process representative of the first class of embodiments. Step 14 represents the step of selecting the substrate plastic for the application in which the tag will be used. The substrate is preferably sized so as to be the largest size that will fit within flat panel display manufacturing equipment that will be used to perform the deposition, photolithography, etching and excimer ~~ecimer~~ laser crystallization and annealing steps to be described subsequently. The thickness and material of the substrate is picked with an eye toward the eventual service the integrated circuit formed thereon will be asked to perform and the environment in which it will perform said service. The term "large size" as used in the substrate is meant to indicate such a plastic substrate which can be processed by the flat panel display manufacturing machines. In this particular case, PET has been selected. Typical thickness for the substrate is from 0.1 to 0.25 millimeters. Sizes of the substrates that can be processed in the flat panel display manufacturing machines are constantly increasing, and the large size substrate picked is intended to mean the largest size which flat panel display manufacturing machines of the most current generation can handle, or sizes which earlier generations of flat panel display manufacturing machines (which will be cheaper to acquire) can handle.

Please amend the paragraph from page 12, line 9 as follows:

The key to avoiding reliability problems caused by differential thermal expansion is to coat the plastic substrate with a layer of silicon nitride (hereafter

nitride) or silicon dioxide (hereafter oxide) or other material at a predetermined thickness to get matching strain values between the plastic substrate and the coating layer. The thickness of the nitride or oxide layer 12A and 12B in Figure 1 must be selected such that the "strain" (the amount of deformation under thermal stress) in the oxide or nitride layer substantially (within 5-10%) or exactly matches the corresponding strain of the substrate 10 at the temperature of the operating environment given the geometry and material of the plastic substrate. Also, the oxide or nitride must be applied to both sides of the plastic substrate ~~substate~~ to avoid bowing the substrate at temperature.

Please amend the paragraph from page 21, line 21 as follows:

Step 50 represents the step of depositing a layer of "contact metallization conductor". As used in the claims, this term means depositing a layer of conductor which is usually metal but which could also be other conductors and which fills the via holes to form contacts 52 and 54 to the source and drain regions S and D in Figure 1 and contact 58 to the gate and which covers the areas between devices so that it can be etched into a metallization pattern which connects the devices together appropriately to accomplish the desired function for the integrated circuit. Although the gate contact is shown extending up through another insulation layer 60 that covers the antenna contact leader lines 62 and 64, in reality, the gate contact metalization usually extends on top of insulation layer 44 over to another transistor source, gate or drain contact to implement the tag transceiver circuit. Step 56 represents photolithographically etching the metal layer to form the contact metallization pattern that ~~the~~ connects the ~~varius~~ various transistors of the tag transceiver together.

Please amend the paragraph starting at page 29, line 14 as follows:

Figure 7 is a process flow for a process to manufacture the EEPROM structure shown in Figure 8. The steps of Figure 7 that are identical to process steps of Figure 2 or Figure 4 are performed with any of the process steps defined above to accomplish the desired result or equivalents. The other steps which are not present in either Figure 2 or Figure 4 are performed with the same processes described above for deposits and etching of metal and oxide layers. Considering Figures 7 and 8 together ~~togethr~~, step 156 represents selection of the substrate material for substrate 154. Step 156 represents the deposition of the nitride or oxide layers 158A and 158B to the proper thicknesses to eliminate or reduce differential strain at the anticipated operating temperature and/or, in some embodiments, to protect the substrate from the strong acids and bases and etchants of subsequent processing steps. Step 162 represents the process of depositing amorphous silicon layer 162. Step 164 represents the optional excimer laser pulse heating of the amorphous silicon layer to crystallize it into polysilicon or microcrystalline silicon. Step 166 is a PECVD deposition of gate oxide layer 168 below floating gate 170. In some embodiments, nitride could also possibly be used. In processes to build integrated circuits that include plain MOS transistors in addition to EEPROM cells, step 166 will typically be accomplished by masking off areas where MOS transistors are being formed to expose areas where EEPROM memory cells are to be formed. Then one or more layers of gate insulator are deposited by PECVD to form an insulation layer that is to lie below the floating gate, where the thickness and materials selected for said one or more layers of gate insulator are such as to achieve Fowler-Noordheim tunnelling to the floating gate from a channel region at whatever programming voltage can be achieved on said integrated circuit. Programming voltages at about 5 volts or

below have been recently achieved in EEPROMs and may continue to descent. Programming voltages on active tags can be higher by virtue of the presence of a battery than can be achieved on passive tags. The PECVD deposition is accomplished at a temperature below the glass transistion temperature of said plastic substrate.